Orca: A Bottom-Up Verification Framework for Systems Software

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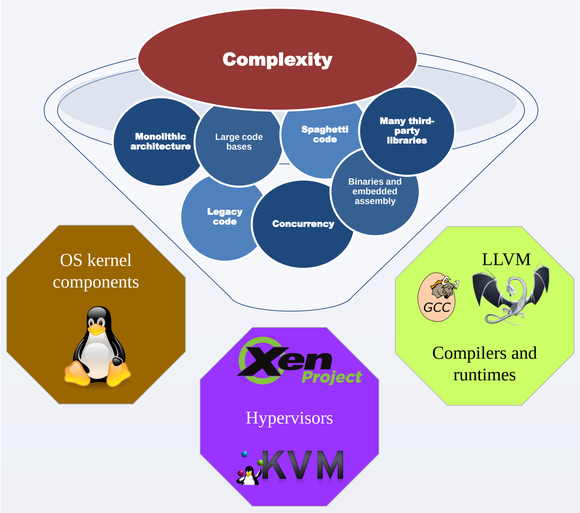
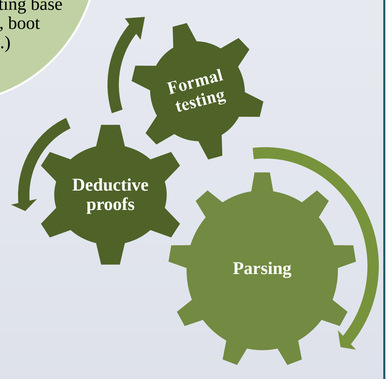
SYSTEMS SOFTWARE

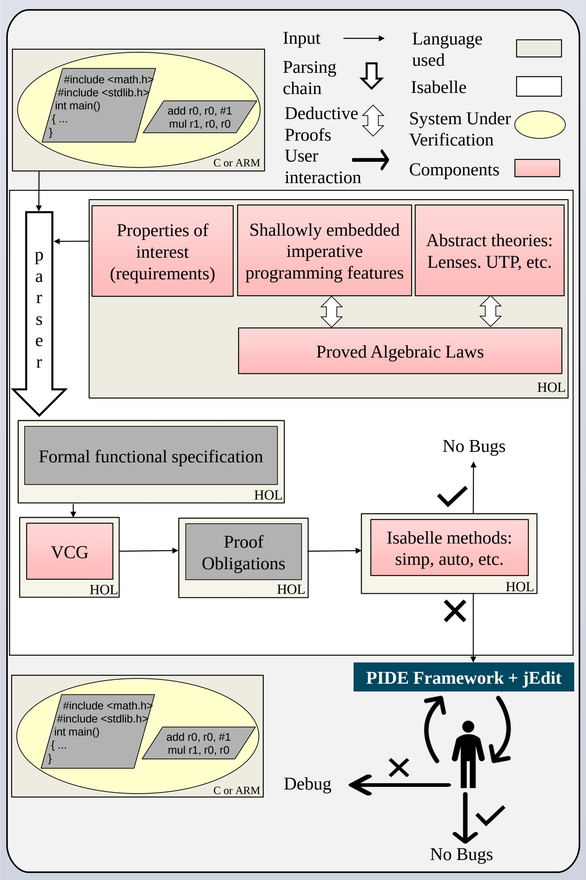


ORCA WORKFLOW

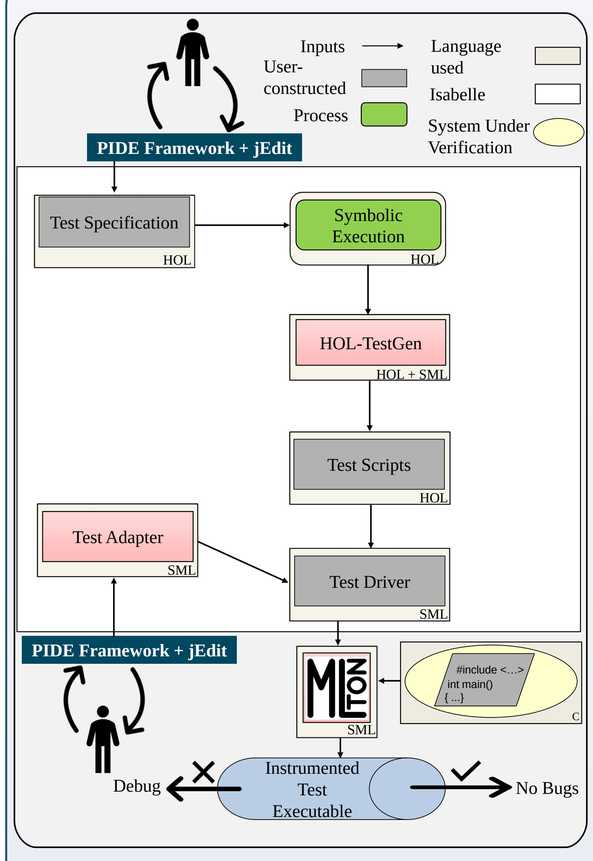
Requirements
- Sophisticated formal behavioral specification and verification techniques covering concurrency, etc.
- Bottom-up approach: scalable verification framework for legacy code.
- Large trusted computing base (compiler, assembler, boot loader, hardware, etc.)

Maximum automation!



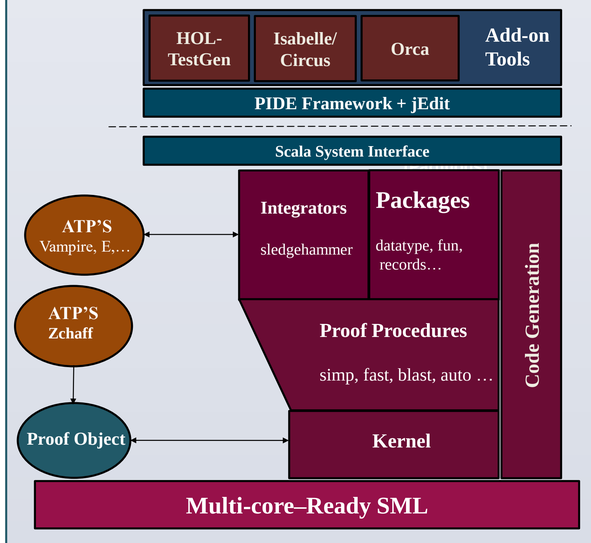


- Isabelle/HOL [10] is extended with formal specifications of a subset of the semantics of C and ARM assembly.
- Then, the parser automatically maps the raw code describing the program to a formal code specification.
- The generated formal specification is then verified using deductive proofs (both automatic and interactive) to ensure full functional correctness.



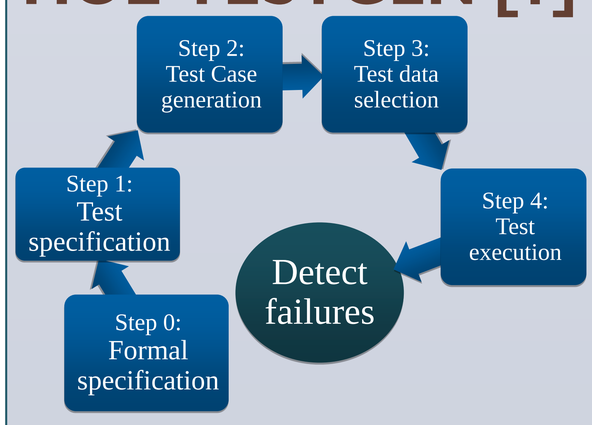
- Deductive proof verification assumes a trusted computing base (TCB) including hardware, compiler, OS, and toolchain.
- The TCB is validated using HOL-TestGen [1].

ISABELLE/HOL [9]



Isabelle
- ✓ Interactive proof assistant.
- ✓ Supports many logics (FOL, HOL, ZF).
- ✓Supports many specification constructs.
- ✓Provides tools for proof automation.

HOL-TESTGEN [1]



HOL-TestGen
- ✓Built on top of Isabelle/HOL.
- ✓Provides modeling environment for test theory.
- ✓Supports transformation of test specifications.
- ✓Supports test generation process.

STATE OF THE ART [7]

- Limited to 10kLOC.
- TCB is hard to justify.
- Has difficulty formally describing behaviors.

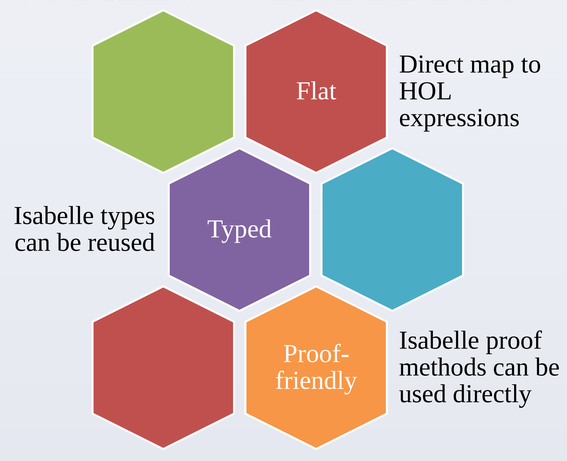
DESIGN CHOICES

Shallow embedding for semantics

State space specified via lenses [3]

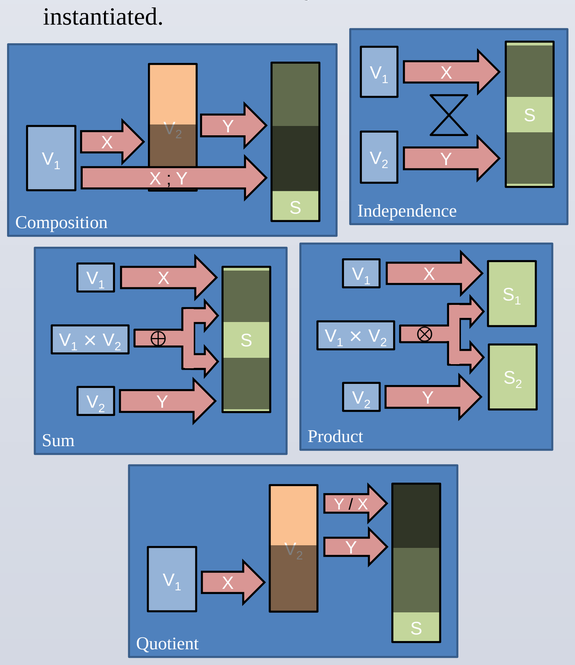
Statements specified via Unifying Theories of Programming (UTP) [2, 6]

SHALLOW EMBEDDING

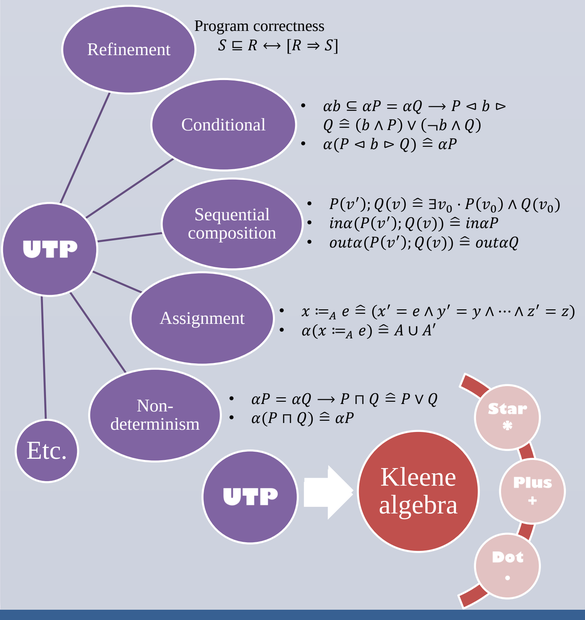


LENSES [2]

- Solve complex data structure problem (structs, unions).
- Allows an abstract memory model that can be later instantiated.



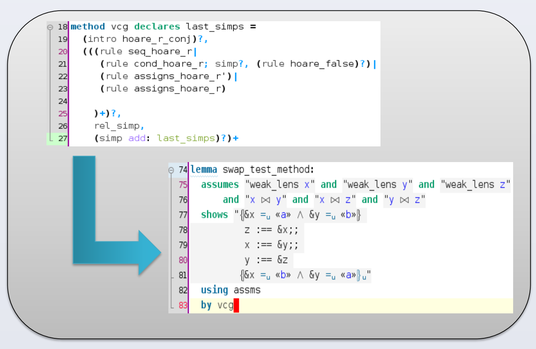
UTP [2]



VERIFICATION CONDITION GENERATOR

- Based on rules of Hoare logic [4] and algebraic laws of programming [5].
- Hoare notation: {pre-condition}program{post-condition}
- Implementation via Eisbach methods [8] and ML-level tactics.

SKIP	• $\{P\}SKIP\{P\}$
ASN	• $\{P[a/x]\}x := a\{P\}$
SEQ	• $\{P\}C_1\{Q\} \Rightarrow \{Q\}C_2\{R\} \Rightarrow \{P\}C_1; C_2\{R\}$
COND	• $\{P \wedge b\}C_1\{Q\} \Rightarrow \{P \wedge \neg b\}C_2\{Q\} \Rightarrow \{P\}C_1 \lhd b \rhd C_2\{Q\}$
WHILE	• $\{P \wedge b\}C\{P\} \Rightarrow \{P\}WHILE\ b\ DO\ C\ OD\{P \wedge \neg b\}$
PRE/POST	• $P \longrightarrow P' \Rightarrow \{P'\}C\{Q\} \Rightarrow \{P\}C\{Q\}$ • $Q' \longrightarrow Q \Rightarrow \{P\}C\{Q'\} \Rightarrow \{P\}C\{Q\}$
MISC	• $\{P\}C\{true\}$ • $\{false\}C\{Q\}$ • $\{P\}C\{Q\} \Rightarrow \{P\}C\{R\} \Rightarrow \{P\}C\{Q \wedge R\}$



CURRENT STATUS

- ✓ UTP specification extended
- ✓ VCG development nearing completion
- ✓ Test specifications in planning stage

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